IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Akhil K. Garlapati et al.		
Title:	VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA EFFECT OF A CMOS BIPOLAR TRANSISTOR		
Application No.:	10/813,837	Filed:	March 31, 2004
Examiner:	Rajnikant B. Patel	Group Art Unit:	2838
Atty. Docket No.:	026-0044	Confirmation No.:	6047

March 2, 2007

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SUPPLEMENTAL RESPONSE AFTER FINAL REJECTION (37 C.F.R. § 1.116)

This paper is being submitted following a final Office action, mailed September 29, 2006, a Response After Final Rejection, filed on November 29, 2006, an Advisory Action, mailed January 3, 2007, and a Notice of Appeal, filed January 9, 2007. In light of the Amendments and/or Remarks herein, further consideration is requested.

Applicant has previously extended the period for filing a response to the final Office action by one month from the mailing date of the Advisory Action. Therefore the remaining fee amount under 37 CFR 1.17(a) to extend the period for reply for a total of two months from the mailing date of the Advisory Action is $330. Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 50-0631.